nitride-aluminum oxide, oxide-aluminum oxide-oxide, oxide-silicon oxycarbide-oxide, composite layers of an oxide-an oxide of Ti, Ta, Hf, Zr, or La, and an oxide, composite layers of an oxide-a non-stoichiometric oxide of Si, N, Al, Ti, Ta, Hf, Zr, and La, and an oxide, composite layers of an oxide-a wet oxide not annealed, and an oxide, composite layers of an oxide-a silicon rich oxide, and an oxide, composite layers of an oxide-a silicon rich aluminum oxide, and an oxide, and composite layers of an oxide-a silicon oxide with silicon carbide nanoparticles, and an oxide.

24. The method of claim 22, wherein forming a tunnel insulator on the surface of the first sidewall, forming a trapping layer on the tunnel insulator, forming a first insulator as an intergate insulator over the trapping layer, and forming a first control gate over the first insulator, and on the surface of the second sidewall forming a second insulator and forming a second control gate over the second insulator further comprises first forming a tunnel insulator on the surface of the first sidewall and forming a trapping layer on the tunnel insulator, then forming the first and second insulators over the trapping layer and on the surface of the second sidewall, and forming the first and second control gates over the first and second insulators, wherein each layer is deposited over the two raised areas and trench, masked, and directionally etched.

TH 8/4/05

25. A method of forming ~~a floating gate~~ an NROM memory array, comprising:

forming a plurality of pillars and associated intervening trenches on a substrate by depositing a layer of masking material, patterning the masking material, and anisotropically etching the substrate; and

forming a plurality of NROM memory cell structures, each NROM memory cell structure having a trapping layer and a coupled select gate, where each NROM memory cell structure is formed by,

depositing a layer of tunnel insulator material over two pillars and an intervening trench;